FLASH MEMORY CELL HAVING REDUCED LEAKAGE CURRENT

ABSTRACT OF THE DISCLOSURE

A flash memory cell of the present invention comprises a floating gate, having a charge trapping region and a fin region. A source region and a drain region is formed proximate the floating gate. A control gate is formed above the charge trapping region of the floating gate. The fin region advantageously reduces leakage current, thereby allowing further scaling of the cell.